

Application No. 09/777,003
Amendment dated January 20, 2004
Reply to Office Action of August 21, 2003

Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (previously amended) An integrated multimedia system having a multimedia processor disposed in an integrated circuit, said system comprising:

a first host processor system coupled to said multimedia processor;

a second local processor disposed within said multimedia processor for controlling the operation of said multimedia processor;

a data transfer switch disposed within said multimedia processor and coupled to said second processor for transferring data to various modules of said multimedia processor;

a data streamer coupled to said data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within said multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations;

an interface unit coupled to said data streamer having a plurality of input/output (I/O) device driver units;

a multiplexer coupled to said interface unit for providing access between a

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selected number of said I/O device driver units to external I/O devices via output pins; and
a plurality of external I/O devices coupled to said multimedia processor.

¹₂ ²₂₀ (previously added) The system in accordance with claim ¹~~19~~, wherein said
external I/O devices are controlled by a corresponding one of said I/O device driver units.

³₂₁ (previously added) The system in accordance with claim ²~~20~~, wherein one
of said external I/O device is an NTSC decoder.

⁴₂₂ (previously added) The system in accordance with claim ²~~20~~, wherein one
of said external I/O device is an NTSC encoder.

⁵₂₃ (previously added) The system in accordance with claim ²~~20~~, wherein one
of said external I/O device is a demodulator unit configured to demodulate wireless
communications signals.

⁶₂₄ (previously added) The system in accordance with claim ⁵~~23~~, wherein said
demodulator unit communicates with said multimedia processor in accordance with a transport
channel interface arrangement.

⁷_{25.} (previously added) The system in accordance with claim ²₂₀, wherein said multimedia processor provides video signals and three dimensional graphic signals to an external video display device.

⁸_{26.} (previously added) The system in accordance with claim ²₂₀, wherein one of said external I/O device is an ISDN interface.

⁹_{27.} (previously added) The system in accordance with claim ²₂₀, wherein one of said external I/O device is an audio coder and decoder (CODEC) unit.

¹⁰_{28.} (previously amended) An integrated multimedia system having a multimedia processor disposed in an integrated circuit, said system comprising:

- a processor disposed within said multimedia processor for controlling the operation of said multimedia processor;
- a data transfer switch disposed within said multimedia processor and coupled to said processor for transferring data to various modules of said multimedia processor;
- a data streamer coupled to said data transfer switch, ⁶²_{and} configured to schedule simultaneous data transfers among a plurality of modules disposed within said multimedia processor, at least one of which is a cache memory, in accordance with corresponding channel allocations;

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an interface unit coupled to said data streamer having a plurality of
input/output (I/O) device driver units;

a multiplexer coupled to said interface unit for providing access between a
selected number of said I/O device driver units to external I/O devices via output pins; and
a plurality of external I/O devices coupled to said multimedia processor.

¹¹
~~28.~~ (previously added) The system in accordance with claim ¹⁰~~28~~, wherein said
external I/O devices are controlled by a corresponding one of said I/O device driver units.

¹²
~~29.~~ (previously added) The system in accordance with claim ¹¹~~29~~, wherein one
of said external I/O device is an NTSC decoder.

¹³
~~31.~~ (previously added) The system in accordance with claim ¹¹~~31~~, wherein one
of said external I/O device is an NTSC encoder.

¹⁴
~~32.~~ (previously added) The system in accordance with claim ¹¹~~32~~, wherein one
of said external I/O device is a demodulator unit configured to demodulate wireless
communications signals.

¹⁵
~~33.~~ (previously added) The system in accordance with claim ¹⁴~~33~~, wherein said

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demodulator unit communicates with said multimedia processor in accordance with a transport channel interface arrangement.

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34.

(previously added) The system in accordance with claim ~~29~~¹¹, wherein said

multimedia processor provides video signals and three dimensional graphic signals to an external video display device.

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35.

(previously added) The system in accordance with claim ~~29~~¹¹, wherein one

of said external I/O device is an ISDN interface.

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36.

(previously added) The system in accordance with claim ~~29~~¹¹, wherein one

of said external I/O device is an audio coder and decoder (CODEC) unit.

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37.

(previously amended) The system in accordance with claim ~~19~~¹, further

comprising a cache memory directly coupled to said second local processor and said data transfer switch.

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38.

(previously added) The system in accordance with claim ~~28~~¹⁰, wherein said

cache memory is directly coupled to said processor and said data transfer switch.

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39. (currently amended) The system in accordance with claim 19, wherein
said plurality of modules among which said data streamer configures to schedule simultaneous
data transfers include the interface unit which is capable of controlling the external I/O devices,
and a memory controller which is capable of controlling an external memory[, and the cache
memory coupled to said second processor].


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40. (currently amended) The system in accordance with claim 28, wherein
said plurality of modules among which said data streamer configures to schedule simultaneous
data transfers include the interface unit which is capable of controlling the external I/O devices,
and a memory controller which is capable of controlling an external memory[, and the cache
memory coupled to said second processor].

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41. (currently amended) The system in accordance with claim 29, wherein
said plurality of modules among which said data streamer configures to schedule simultaneous
data transfers further include another interface unit which is capable of controlling said first
processor.

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42. (currently amended) The system in accordance with claim 40, wherein
said plurality of modules among which said data streamer configures to schedule simultaneous
data transfers further include another interface unit which is capable of controlling [said] a first

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host processor.

 ~~25~~
~~43.~~ (previously added) The system in accordance with claim ~~19~~¹, wherein said
data transfer switch further comprises a plurality of buses.

~~26~~
~~44.~~ (previously added) The system in accordance with claim ~~28~~¹⁰, wherein said
data transfer switch further comprises a plurality of buses.
